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Description

The present invention relates to a photoelectric converting apparatus of the type having a plurality of photosensors and a plurality of signal output lines for picking up signals from the photosensors, wherein the signals are picked up through signal output terminals smaller in number than that of the signal output lines.

Related Background Art

In order to read signals from the entirety or part of a color sensor made of a plurality of photosensors disposed one or two-dimensionally, it becomes necessary to provide a plurality of signal output lines.

Fig. 1 is a circuit diagram showing one example of a conventional photoelectric converting apparatus.

In the Figure, there are provided sensor line blocks 101 and 102 each constructed of one-dimensionally disposed photosensors. Signals from each sensor line block is sequentially read via signal output lines 103 and 104 which are commonly connected to an amplifier 105 having a signal output terminal 106. During reading signals from one sensor line blocks, reading signals from the other line sensor block is inhibited. Thus, signals from the two signal output lines can be read via the single output terminal, resulting in less number of wirings to external circuitry.

In operation of the above conventional photoelectric converting apparatus, signal from the sensor line blocks 101 and 102 are temporarily stored in charge storage capacitors or wiring capacitance C1 to Cn. Signals from the sensor line blocks 101 and 102 are sequentially picked up to the signal output lines 103 and 104, respectively under control of shift registers. The signals are then outputted via the amplifier 105 at its signal output terminal 106.

However, since the signal output lines 103 and 104 are connected together at the input terminal of the amplifier, each wiring capacitance Cw1 and Cw2 of the signal output line are added together, resulting in a large capacitance of each signal output line. Thus, there arises a problem that the output of a signal stored, for example, in the charge storage capacitor C1 is reduced at the signal output line 103 by the large capacitance.

The above problem becomes more serious in the case of a large number of sensor lines and hence a large number of signal output lines.

There is known from JP-A-59-154879 a photoelectric conversion apparatus in which first and second shift registers are provided, the outputs of which are connected via a switch to a common amplifier and video output terminal. One of the shift registers may be connected to the amplifier and its output scanned out, and then the switch means can connect the other shift register to the amplifier so that its output can be scanned out.

JP-A-61-82585 discloses a system in which a series of buffer amplifiers are connected in parallel, each with a respective input capacitance and respective output capacitance, and the outputs of the buffer amplifiers and their respective output capacitances are connected through switch means to a common output terminal.

SUMMARY OF THE INVENTION

According to the present invention there is provided photoelectric conversion apparatus as set out in claim 1 and an operating method as set out in claim 8. The remaining claims set out optional features.

An embodiment of the present invention provides a photoelectric converter with less reduction in signal output level.

An embodiment of the present invention provides an image pickup apparatus suitable for high resolution.

In an embodiment of the invention a photoelectric converting apparatus has a plurality of photosensors and a plurality of signal output lines for picking up signals from the photosensors, wherein the signals are picked up through signal output terminals smaller in number than that of the signal output lines, and the signal output lines each have switch means for switching the signal output lines and connecting a desired output line to a signal output terminal.

Since a plurality of selection means (scanning circuits such as shift registers) are provided, the drive frequency of selection means may use a lower frequency in cases where a high frequency operation becomes necessary for a great number of photosensors, thus enabling a high degree of freedom in circuit design, pattern design for semiconductor devices and the like.

Since each signal output line is connected to the signal output terminal via switch means, the wiring capacity of the signal output line from which a signal is picked up via the closed switch means can be greatly reduced by opening the other switch means. Therefore, reduction in signal level at the signal output line can be avoided, and an image pickup apparatus with a high resolution and high output can be easily realized.

Other objects and advantages of the present invention will become apparent from the following description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram showing an example of a conventional photoelectric converting apparatus;

Fig. 2A is a schematic circuit diagram showing an

embodiment of the photoelectric converting apparatus according to the present invention;

Fig. 2B is a schematic cross section of a photoelectric conversion cell disclosed in Japanese Patent Laid-open Gazettes Nos. 12579/1985 and 12765/1985;

Fig. 2C is a equivalent circuit of the photoelectric conversion cell shown in Fig. 2B;

Fig. 3A is a circuit diagram showing an example of a driver for a sensor line block using the photoelectric conversion cells of Fig. 2B;

Fig. 3B is a timing chart for explaining the operation of the circuit shown in Fig. 3A;

Fig. 4 is a block diagram showing an example of an image pickup apparatus using the embodiment of Fig. 3A;

Fig. 5 is a schematic circuit diagram showing an embodiment of the photoelectric converting apparatus according to the present invention;

Fig. 6 is a timing chart for explaining the operation of the scanning circuit; and

Figs. 7 is a timing chart showing an example of timings of pulses outputted from the driver 117.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The embodiments of the present invention will be described in detail with reference to the accompanying drawings.

Fig. 2A is a schematic circuit diagram showing an embodiment of the photoelectric converting apparatus according to the present invention.

In the Figure, a signal output line 103 from which signals from a sensor line block 101 are sequentially outputted is connected to the input terminal of an amplifier 105 via switch means 107. Similarly, a signal output line 104 from which signals from a sensor line block 102 are sequentially outputted is connected to the input terminal of the amplifier 105 via switch means 108.

MOS transistors are used as switch means in this embodiment. However, other devices having a low conductive resistance such as analog switches may obviously be used.

Also, instead of two signal output lines, a larger number of signal output lines may be commonly connected to the input terminal of the amplifier 105 via switch means.

In operation of this embodiment, while signals from the sensor line block 101 are sequentially outputted to the signal output line 103 by means of a shift register 115, switch means 107 is kept turned on and switch means 108 is kept turned off. Therefore, the wiring capacitance of the signal output line becomes substantially the wiring capacitance Cw1 of the signal output line 103 alone. Thus, if each capacitance C of charge storage capacitors C1 to Cn is set sufficiently large as compared with Cw1, then it becomes possible to read signals from sensors without reducing their signal level.

Conversely, while signals from the sensor line block 102 are read by means of a shift register 116, switch means 107 is kept turned off whereas switch means 108 is kept turned on. Similarly in this case, signals can be read without reducing their signal level.

Next, the structure and operation of the line sensor block in this embodiment will be described in more particular.

Fig. 2B is a schematic cross section of a photoelectric conversion cell disclosed in Japanese Patent Laid-open Gazettes Nos. 12759/1985 and 12765/1985, and Fig. 2C is an equivalent circuit of the photoelectric conversion cell.

In the Figures, each photosensor cell is formed on an n^+ silicon substrate 1 and electrically isolated from adjacent photosensor cells by an element isolation region 2 made of, for example, SiO_2, Si_3N_4, polysilicon or the like.

Each photosensor cell has the following constituent elements: A p-region 4 is formed by doping p-type impurity on an n^--region 3 of low impurity concentration formed by the epitaxy method or the like. An n^+-region 5 is formed in the p-region 104 by the impurity diffusion method, the ion implantation method or the like. The p-region 4 and n^+-region 5 serve as the base and emitter of a bipolar transistor, respectively.

Formed on an oxide film 6 deposited on the n^--region 3 with the above regions is a capacitor electrode 7 of predetermined area which faces the p-region 4 with the oxide film 6 interposed therebetween. The potential of the p-region 104 in a floating state is controlled by a pulse voltage applied to the capacitor electrode 7.

The photosensor cell is constructed further of an emitter electrode 8 connected to the n^+-region 5, an n^+-region 11 of high impurity concentration formed on the substrate 1, and an electrode 12 supplying a potential to the collector of the bipolar transistor.

Next, the fundamental operations of the photosensor constructed as above will be described. First, assuming that the p-base region 4 of the transistor is at a negative potential and at a floating state. Upon incidence of light 13 to the p-region 4, holes of light-induced electron/hole pairs are accumulated in the p-region 4 the potential of which rises positively due to the accumulated holes (accumulation operation).

Next, a readout positive pulse is applied to the capacitor electrode 7 so that a readout signal corresponding to a change in base potential during the accumulation operation is outputted from the emitter electrode (readout operation). Repetitive readout operations are possible because the accumulated charge amount in the base p-region 4 does not de-

crease to large extent.

To remove accumulated holes in the p-region 4, the emitter electrode 8 is grounded and the capacitor electrode 8 is applied with a positive refresh pulse. With this pulse applied, the p-region 4 is forward biased relative to the n^+ region 5 so that accumulated holes are removed. At the trailing edge of the refresh pulse, the p-region 4 takes again its initial negative potential (refresh operation). Thereafter, similar accumulation, readout and refresh operations are repeated.

Briefly stating the above proposed method, light-induced carriers are accumulated in the base p-region 4 to control a current passing through the emitter and collector electrodes 8 and 12 in accordance with the accumulated charge quantity. The accumulated carriers are read after amplifying them by the amplification function of each cell, thereby achieving a high output and sensitivity, and less noises.

The potential V_p of the base with light-induced carriers (holes in this case) accumulated therein is given by Q/C, wherein Q represents the charge of carriers accumulated in the base region, and C represents a capacitor coupled to the base region. As apparent from the above equation, the values of Q and C both become small as the cell size becomes small due to high integration. Thus, the light-induced potential Vp is maintained substantially constant. Therefore, the above proposed method may become useful in the future for a means of obtaining a high resolution.

Fig. 3A is a circuit diagram showing an example of a driver for the sensor line block using the above photoelectric conversion cells, and Fig. 3B is a timing chart for explaining the operation of the driver circuit.

Referring to Fig. 3A, each collector electrode 12 of the photoelectric conversion cells S1 to Sn is applied with a predetermined voltage. Capacitor electrodes 7 are connected in common to a terminal 110 to which a signal ϕ_1 for the readout and refresh operations is applied. Each emitter electrode 8 is connected to respective vertical lines L1 to Ln which are connected to one main electrodes of respective buffer transistors Ta1 to Tan.

The gate electrodes of the buffer transistors Ta1 to Tan are connected in common to a terminal 111 to which a signal ϕ_2 is applied. The other main electrodes of the buffer transistors Ta1 to Tan are grounded via charge storage capacitors C1 to Cn serving as accumulation means, and also connected to the signal line 103 via transistors T1 to Tn. The gate electrodes of the transistors T1 to Tn are respectively connected to the parallel output terminals of the shift register from which signals ϕh1 to ϕhn are sequentially outputted.

The signal output line 103 is grounded via transistor Tr for refreshing the signal output line 103. The gate electrode of the transistor Tr is applied with a signal ϕ_{r2}.

The vertical lines L1 to Ln are grounded via respective buffer transistors Tb1 to Tbn. The gate electrodes of the buffer transistors Tb1 to Tbn are connected in common to a terminal 112 to which a signal ϕ_3 is applied.

Next, the operation of the embodiment constructed as above will be described with reference to the timing chart shown in Fig. 3B.

Refresh Operation

First, signals ϕ_2 and ϕ_3 are made high level to cause the buffer transistors Ta1 to Tan to turn on. Therefore, the emitter electrodes 8 of the photoelectric conversion cells S1 to Sn are grounded and residual charges in the charge storage capacitors C1 to Cn are removed therefrom. When signal ϕ_1 becomes high level to apply a positive refresh voltage to the capacitor electrode 7 of each photoelectric conversion cell, a refresh operation is performed as described before. When signal ϕ_1 becomes low level, the base region 4 of each cell returns to its intial negative potential.

Accumulation Operation

Signals ϕ_2 and ϕ_3 are made low level to cause the buffer transistors Ta1 to Tan and Tb1 to Tbn to turn off. In this condition, holes of light-induced electron/hole pairs are accumulated in the base region 4 of each photoelectric conversion cell S1 to Sn so that the base potential of each cell rises to a higher value from the initial negative potential by the accumulated potential corresponding to the incident light amount.

Readout Operation

When signals ϕ_1 and ϕ_2 are made high level, signals read from the emitter electrodes 8 of the photoelectric conversion cells S1 to Sn are accumulated at the same time in the charge storage capacitors C1 to Cn via the buffer transistors Ta1 to Tan.

Succeedingly, after signals ϕ_1 and ϕ_2 are made low level, a readout operation for each signal from the signal output line 103 starts.

First, when high level signal ϕh1 is outputted from the shift register, the transistor ϕT1 is caused to turn on. Then, a signal of the photoelectric conversion cell S1 stored in the charge storage capacitor C1 appears on the signal output line 103, and read out from the signal output terminal 106 via switch means 107 and the amplifier 105 as described previously.

Succeedingly, signal ϕ_{r2} is made high level to cause the transistor Tr to turn on. Thus, residual charge on the signal output line 103 is removed via the transistor Tr to effect a refresh operation.

Thereafter, high level signals ϕh2 to ϕhn are se-

quentially outputted in a similar manner as above to cause the transistors to sequentially turn on. Thus, signals stored in the charge storage capacitors C2 to Cn are sequentially outputted on the signal output line 103. Each time after signal has been outputted to the external circuit, signal ϕ_{r2} is made high level to refresh the signal output line 103.

After all the signals stored in the charge storage capacitors C1 to Cn have been read out to the external circuit, the above-described refresh operation is carried out, and the similar accumulation and readout operations follow.

While the sensor line block 101 is read, switch means 107 is turned on and switch means 108 is turned off. Conversely, while the sensor line block 102 is read, switch means 107 is turned off and switch means 108 is turned on.

The type of photosensors is not limited to the above embodiment but the photosensors such as photoconductive type sensors, photodiodes, static induction transistors may be used.

Fig. 4 is a block diagram showing an example of an image pickup apparatus using the above embodiment. In this case, it is needless to say that a number of sensor line blocks are provided and switch means is provided for each sensor line block.

In the Figure, an image pickup device 301 has a similar construction as of the above embodiment. The output signal Vo therefrom is processed including a gain adjustment by a signal processing circuit 302 to output it as a standard television signal in the form of NTSC signal or the like.

Various types of pulses for driving the image pickup device 301 are supplied from a driver 303 which is controlled by a control unit 304. The control unit 304 adjusts a gain and the like of the signal processing circuit 302 in accordance with an output from the image pickup device, and adjusts the incident light amount to the image pickup device 301 by controlling an exposure control unit 305.

As described in detail, each signal output line of the photoelectric converter of the above embodiment according to the present invention is coupled to the output terminal via switch means. Therefore, a wiring capacitance on a signal output line from which a signal is outputted via closed switch means is greatly reduced as compared with a conventional one, by opening switch means on the other signal output lines. Hence, it is possible to prevent lowering the level of a signal outputted from the signal output line.

Next, a second embodiment of the present invention will be described in detail with reference to the associated drawings.

Fig. 5 is a schematic circuit diagram showing an embodiment of the photoelectric converter according to the present invention.

In this embodiment, there are provided sensor line blocks 101 and 102 each having a plurality of n photosensors. Each sensor line block is intended herein to include such concept as it represents odd/even lines of a sensor group such as an area sensor, it represents odd/even photosensors on an arbitrary line, and the like. In this embodiment, for the purpose of convenience of description, two sensor blocks are shown.

In the Figure, n output terminals of the sensor line block 101 are connected to capacitors C11 to C1n and connected in common to a signal output line 103 via transistors T11 to T1n. Each gate electrode of transistor T11 to T1n is inputted with pulses ϕ_{11} to ϕ_{1n} from a scanning circuit 115. Pulses ϕ_{31} and ϕ_{32} are inputted to input terminal a and b of the scanning circuit 115.

The signal line 103 is grounded via transistor Tr1 and connected to the input terminal of an amplifier 105 via a transistor 107 serving as switch means. A pulse ϕ_{c1} is inputted to the gate electrode of the transistor Tr1, and a pulse ϕ_{sr1} is input to the gate electrode of the transistor 107.

The sensor line block 102 is constructed in a similar manner. N output terminals of the sensor line block 102 are connected to capacitors C21 to C2n and connected in common to a signal output line 104 via transistors T21 to T1n. Each gate electrode of transistor T21 to T2n is inputted with pulse ϕ_{21} to ϕ_{2n} from a scanning circuit 116. Pulses ϕ_{32} and ϕ_{31} are inputted to inputted to input terminal a and b of the scanning circuit 116, as opposed to the case of the scanning circuit 115.

The signal line 104 is grounded via transistor Tr2 and connected to the input terminal of the amplifier 105 via a transistor 108 serving as switch means. A pulse ϕ_{c2} is inputted to the gate electrode of the transistor Tr2, and a pulse ϕ_{sr2} is inputted to the gate electrode of the transistor 108.

The operation of the scanning circuits 115 and 116 of this embodiment is as follows.

Fig. 6 is a timing chart illustrating the operation of the scanning circuit.

The scanning circuits 115 and 116 are two-phase driven by pulses ϕ_{31} and ϕ_{32}. With the interconnection shown in Fig. 5, pulses ϕ_{11} to ϕ_{1n} are outputted from the scanning circuit 115 in synchro with the pulse ϕ_{31}, whereas pulses ϕ_{21} to ϕ_{2n} are outputted from the scanning circuit 116 in synchro with the pulse ϕ_{32}, respectively as shown in the timing chart. Therefore, based on the timings of pulses ϕ_{31} and ϕ_{32}, the scanning circuits 115 and 116 can independently or alternately be operated at desired timings.

The above-described various pulses are supplied from a driver 117 which outputs a pulse at the timing in synchro with a clock signal from an oscillator 118.

Transistors 107 and 108 are used as switch means in this embodiment. However, obviously other devices having a low conductive resistance such as analog switches may be used similar to the embodiment shown in Fig. 2.

It is to be understood that the invention includes the arrangement wherein three or more sensor line blocks are provided and the signal output lines are connected in common to the input terminal of the amplifier 109 via respective switch means.

Next, the operation of this embodiment will be described with reference to Fig. 7 which shows a timing chart illustrating an example of timings of pulses outputted from the driver 117.

In the Figure, first, pulse ϕ_{sr1} is made high level and pulse ϕ_{sr2} is made low level to turn on the transistor 107 and turn off the transistor 108.

In this condition, pulse ϕ_{11} is outputted from the scanning circuit 115 to turn on the transistor T11. Thus, a signal at the first cell of the sensor line block 101 is picked up from the capacitor C11 onto the signal output line 103, and hence to the external circuit via the transistor 107, the amplifier 105 and the output terminal 106.

Simultaneously with the pulse ϕ_{11}, pulse ϕ_{c2} is made high level to turn on the transistor Tr2 so that residual charge on the signal output line 104 is removed.

After the signal at the first cell of the sensor block 101 has been outputted, then pulses ϕ_{sr1} and ϕ_{sr2} are inverted respectively to low level and high level to turn off the transistor 107 and turn on the transistor 108.

In this condition, pulse ϕ_{21} is outputted from the scanning circuit 116 to turn on the transistor T21. Then a signal at the first cell of the sensor line block 102 is picked up from the capacitor C21 onto the signal output line 104, and hence to the external circuit via the transistor 108 and the amplifier 105.

Simultaneously with pulse ϕ_{21}, pulse ϕ_{c1} is made high level to turn on the transistor Tr1 and remove residual charge present at the preceding signal on the signal output line 103.

Thereafter, in a similar manner as above, signals from the sensors in the sensor line blocks 101 and 102 are alternately and sequentially outputted to the external circuit in response to pulses ϕ_{12} to ϕ_{1n} from the scanning circuit 115 and pulses ϕ_{22} to ϕ_{2n} from the scanning circuit 116.

It is to be noted that the wiring capacitance on a signal output line from which a signal is read is substantially the wiring capacitance Cw of the line itself because one of the transistors 107 and 108 from which a signal is not read is made turned off. Thus, by seating each capacitance C of the capacitors C11 to C1n and C21 to C2n sufficiently larger than Cw, it becomes possible to read a signal from a cell without greatly reducing its signal level.

Further, since each sensor line block 101 and 102 is provided with respective scanning circuit 115 and 116, the scanning circuit can be driven at a lower operating frequency corresponding to n photosensors although 2n photosensors are used, thus leading to a high degree of freedom in design.

As appreciated from the foregoing detailed description of the photoelectric converting apparatus embodying the present invention, plural number of selection means for selecting photosensors in sensor line blocks are provided. Therefore, even if a high frequency operation is required for a large number of photosensors, selection means can be operated at a lower frequency, resulting in a high degree of freedom in circuit design, pattern design for semiconductor devices, and the like.

Further, each signal output line is connected to the signal output terminal via switch means. During picking up a signal from a signal output line, switch means for this line is closed whereas switch means for the other lines are opened. Therefore, it is possible to prevent lowering the level of a signal picked up from the signal output line, and to readily realize a high resolution and high output image pickup apparatus.

Attention is directed to European divisional application having publication no. EP-A-0 593 139.

Claims

1. Photoelectric conversion apparatus comprising:

   a plurality of sensor blocks (101, 102), each having a plurality of photoelectric conversion cells;

   switch means (107, 108) for directing signals read out from the sensor blocks to a common output terminal (106); and

   read-out control means (303, 304; 117) for controlling the switch means and controlling read-out of signals from the sensor blocks,

   characterised in that the read-out control means has a mode of operation in which it controls the read-out of signals from the sensor blocks in turns, the signals read out in successive turns being from different sensor blocks, to provide a signal from one photoelectric conversion cell per turn and controls the switch means to direct the signals from the sensor blocks in turns to the common output terminal, the signals directed in successive turns being from different sensor blocks, the switch means directing a signal from one photoelectric conversion cell per turn.

2. Apparatus according to claim 1 in which the signals provided to the common output terminal (106) are amplified by a common amplification means (105).

3. Apparatus according to claim 1 or claim 2 further comprising capacitor means (C) for temporarily storing a signal read out from a sensor block (101, 102).

4. Apparatus according to any one of claims 1 to 3 in which each photoelectric conversion cell comprises a bipolar transistor.

5. Apparatus according to any one of the preceding claims in which each said sensor block has an output line (103, 104) having a capacitance (CW1, CW2).

6. Apparatus according to claim 5 in which the switch means (107, 108) is coupled between the output lines (103, 104) and the common output terminal (106) and is arranged so that when the switch means directs a signal which has been read out of a sensor block (101, 102) to the output terminal (106), the output line (103, 104) of that sensor block is coupled to the output terminal (106) and isolated from the output line of another said sensor block.

7. Apparatus according to claim 5 or claim 6 further comprising reset means (Tr) for resetting the common output lines.

8. A method of operating photoelectric conversion apparatus which apparatus comprises a plurality of sensor blocks (101, 102) each having a plurality of photoelectric conversion cells and switch means (107, 108) for directing signals read out from the sensor blocks to a common output terminal (106),

the method being characterised by

reading out signals from the sensor blocks in turns, the signals read out in successive turns being from different sensor blocks, to provide a signal from one photoelectric conversion cell per turn, and switching the switch means to direct the signals from the sensor blocks in turns to the common output terminal, the signals directed in successive turns being from different sensor blocks, the switch means directing a signal from one photoelectric conversion cell per turn.

9. A method according to claim 8 in which the photoelectric apparatus comprises first and second sensor blocks and the signals are read out alternately one from each of the first and second sensor blocks.

10. A method according to claim 8 or claim 9 in which each sensor block (101, 102) has an output line (103, 104), a signal is read out from a first sensor block during a first period, and the output line of the first sensor block is reset and a signal is read out from a second sensor block during a second period.

Patentansprüche

1. Fotoelektrische Umwandlungsvorrichtung enthaltend:

eine Vielzahl von Sensorblöcken (101, 102), von denen jeder eine Vielzahl von fotoelektrischen Umwandlungszellen hat;

eine Schaltvorrichtung (107, 108) zum Zuführen von aus den Sensorblöcken ausgelesenen Signalen zu einem gemeinsamen Ausgabeanschluß (106); und

eine Auslesesteuervorrichtung (303, 304; 117) zum Steuern der Schaltvorrichtung und zum Steuern des Auslesens von Signalen aus den Sensorblöcken,

dadurch gekennzeichnet, daß die Auslesesteuervorrichtung eine Betriebsart hat, in welcher sie das Auslesen der Signale von den Sensorblöcken wechselweise steuert, wobei die in aufeinanderfolgenden Durchgängen ausgelesenen Signale von verschiedenen Sensorblöcken stammen, um pro Durchgang ein Signal von einer fotoelektrischen Umwandlungszelle zu liefern, und die Schaltvorrichtung steuert, um die Signale von den Sensorblöcken wechselweise dem gemeinsamen Ausgabeanschluß zuzuführen, wobei die in aufeinanderfolgenden Durchgängen zugeführten Signale von verschiedenen Sensorblöcken stammen, wobei die Schaltvorrichtung pro Durchgang ein Signal von einer fotoelektrischen Umwandlungszelle zuführt.

2. Vorrichtung nach Anspruch 1, bei welcher die dem gemeinsamen Ausgabeanschluß (106) zugeführten Signale durch eine gemeinsame Verstärkungsvorrichtung (105) verstärkt werden.

3. Vorrichtung nach Anspruch 1 oder Anspruch 2, ferner aufweisend eine Kondensatorvorrichtung (C) zum vorübergehenden Speichern eines von einem Sensorblock (101, 102) ausgelesenen Signals.

4. Vorrichtung nach einem der Ansprüche 1 bis 3, bei der jede fotoelektrische Umwandlungszelle einen bipolaren Transistor aufweist.

5. Vorrichtung nach einem der vorhergehenden Ansprüche, bei der jeder Sensorblock eine Ausgabeleitung (103, 104) mit einer Kapazität (CW1, CW2) hat.

6. Vorrichtung nach Anspruch 5, bei der die Schaltvorrichtung (107, 108) zwischen den Ausgabeleitungen (103, 104) und dem gemeinsamen Ausgabeanschluß (106) gekoppelt und so eingerichtet ist, daß, wenn die Schaltvorrichtung ein von einem Sensorblock (101, 102) ausgelesenes Si-

gnal dem Ausgabeanschluß (106) zuführt, die Ausgabeleitung (103, 104) dieses Sensorblocks zum Ausgabeanschluß (106) gekoppelt und von der Ausgabeleitung eines anderen Sensorblocks isoliert ist.

7. Vorrichtung nach Anspruch 5 oder Anspruch 6, ferner aufweisend eine Rücksetzvorrichtung (Tr) zum Rücksetzen der gemeinsamen Ausgabeleitungen.

8. Verfahren zum Betreiben einer fotoelektrischen Umwandlungsvorrichtung, welche eine Vielzahl von Sensorblöcken (101, 102), von denen jeder eine Vielzahl von fotoelektrischen Umwandlungszellen aufweist, und eine Schaltvorrichtung (107, 108) zum Zuführen von von den Sensorblöcken ausgelesenen Signalen zu einem gemeinsamen Ausgabeanschluß (106) aufweist,

   wobei das Verfahren gekennzeichnet ist durch

   wechselweises Auslesen von Signalen aus den Sensorblöcken, wobei die in aufeinanderfolgenden Durchgängen ausgelesenen Signale von verschiedenen Sensorblöcken stammen, um pro Durchgang ein Signal von einer fotoelektrischen Umwandlungszelle zu liefern, und Schalten der Schaltvorrichtung, um die Signale von den Sensorblöcken wechselweise dem gemeinsamen Ausgabeanschluß zuzuführen, wobei die in aufeinanderfolgenden Durchgängen zugeführten Signale von verschiedenen Sensorblöcken stammen, wobei die Schaltvorrichtung pro Durchgang ein Signal von einer fotoelektrischen Umwandlungszelle liefert.

9. Verfahren nach Anspruch 8, bei dem die fotoelektrische Umwandlungsvorrichtung erste und zweite Sensorblöcke aufweist und die Signale alternierend ausgelesen werden, eines von jedem der ersten und zweiten Sensorblöcke.

10. Verfahren nach Anspruch 8 oder 9, bei dem jeder Sensorblock (101, 102) eine Ausgabeleitung (103, 104) hat, ein Signal von einem ersten Sensorblock während einer ersten Periode ausgelesen wird, und während einer zweiten Periode die Ausgabeleitung des ersten Sensorblocks zurückgesetzt und ein Signal von einem zweiten Sensorblock ausgelesen wird.

Revendications

1. Dispositif de conversion photoélectrique comprenant :

   un ensemble de blocs de capteurs (101, 102), comportant chacun un ensemble de cellules de conversion photoélectrique ;

   des moyens de commutation (107, 108) pour diriger vers une borne de sortie commune (106) des signaux qui sont lus dans les blocs de capteurs ; et

   des moyens de commande de lecture (303, 304 ; 117), pour commander les moyens de commutation et pour commander la lecture de signaux dans les blocs de capteurs,

   caractérisé en ce que les moyens de commande de lecture ont un mode de fonctionnement dans lequel ils commandent la lecture de signaux dans les blocs de capteurs par tours, les signaux qui sont lus au cours de tours successifs provenant de blocs de capteurs différents, pour produire un signal provenant d'une cellule de conversion photoélectrique par tour, et ils commandent les moyens de commutation de façon à diriger vers la borne de sortie commune les signaux qui proviennent des blocs de capteurs par tours, les signaux qui sont dirigés au cours de tours successifs provenant de différents blocs de capteurs, et les moyens de commutation dirigeant un signal à partir d'une seule cellule de conversion photoélectrique par tour.

2. Dispositif selon la revendication 1, dans lequel les signaux qui sont appliqués à la borne de sortie commune (106) sont amplifiés par un moyen d'amplification commun (105).

3. Dispositif selon la revendication 1 ou la revendication 2, comprenant en outre des moyens à condensateur (C) pour stocker temporairement un signal lu dans un bloc de capteurs (101, 102).

4. Dispositif selon l'une quelconque des revendications 1 à 3, dans lequel chaque cellule de conversion photoélectrique comprend un transistor bipolaire.

5. Dispositif selon l'une quelconque des revendications précédentes, dans lequel chaque bloc de capteurs comporte une ligne de sortie (103, 104) ayant une capacité (CW1, CW2).

6. Dispositif selon la revendication 5, dans lequel les moyens de commutation (107, 108) sont connectés entre les lignes de sortie (103, 104) et la borne de sortie commune (106) et ils sont conçus de façon que lorsque les moyens de commutation dirigent vers la borne de sortie (106) un signal qui a été lu dans un bloc de capteurs (101, 102), la ligne de sortie (103, 104) de ce bloc de capteurs soit connectée à la borne de sortie (106) et soit isolée de la ligne de sortie d'un autre bloc de capteurs.

7. Dispositif selon la revendication 5 ou la revendication 6, comprenant en outre des moyens de restauration (Tr) pour restaurer les lignes de sortie communes.

8. Un procédé pour faire fonctionner un dispositif de conversion photoélectrique qui comprend un ensemble de blocs de capteurs (101, 102) ayant chacun un ensemble de cellules de conversion photoélectrique et des moyens de commutation (107, 108) pour diriger vers une borne de sortie commune (106) des signaux qui sont lus dans les blocs de capteurs,
le procédé étant caractérisé par
la lecture, par tours, des signaux provenant des blocs de capteurs, les signaux qui sont lus au cours de tours successifs provenant de blocs de capteurs différents, pour produire un signal provenant d'une seule cellule de conversion photoélectrique par tour, et la commutation des moyens de commutation, de façon à diriger vers la borne de sortie commune les signaux qui proviennent des blocs de capteurs par tours, les signaux qui sont dirigés au cours de tours successifs provenant de blocs de capteurs différents, et les moyens de commutation dirigeant un signal provenant d'une seule cellule de conversion photoélectrique par tour.

9. Un procédé selon la revendication 8, dans lequel le dispositif de conversion photoélectrique comprend des premier et second blocs de capteurs, et les signaux sont lus en alternance à raison d'un signal provenant de chacun des premier et second blocs de capteurs.

10. Un procédé selon la revendication 8 ou la revendication 9, dans lequel chaque bloc de capteurs (101, 102) comporte une ligne de sortie (103, 104), un signal est lu à partir d'un premier bloc de capteurs pendant une première période, et la ligne de sortie du premier bloc de capteurs est restaurée et un signal est lu à partir d'un second bloc de capteurs pendant une seconde période.

FIG. 1

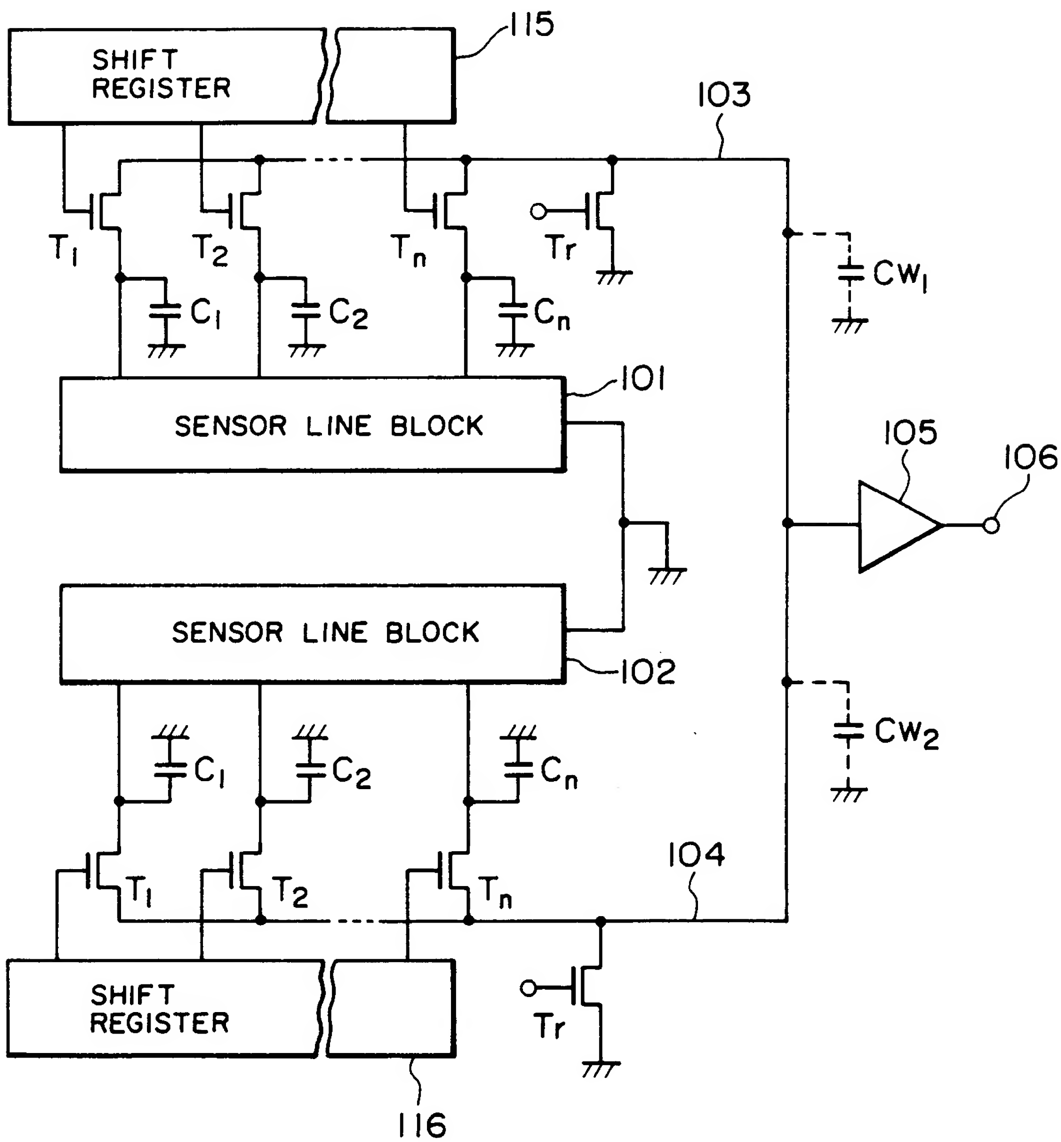

SHIFT REGISTER
115
103
T_1
T_2
T_n
Tr
C_1
C_2
C_n
CW_1
101
SENSOR LINE BLOCK
105
106
SENSOR LINE BLOCK
102
CW_2
C_1
C_2
C_n
104
T_1
T_2
T_n
SHIFT REGISTER
Tr
116

FIG. 2A

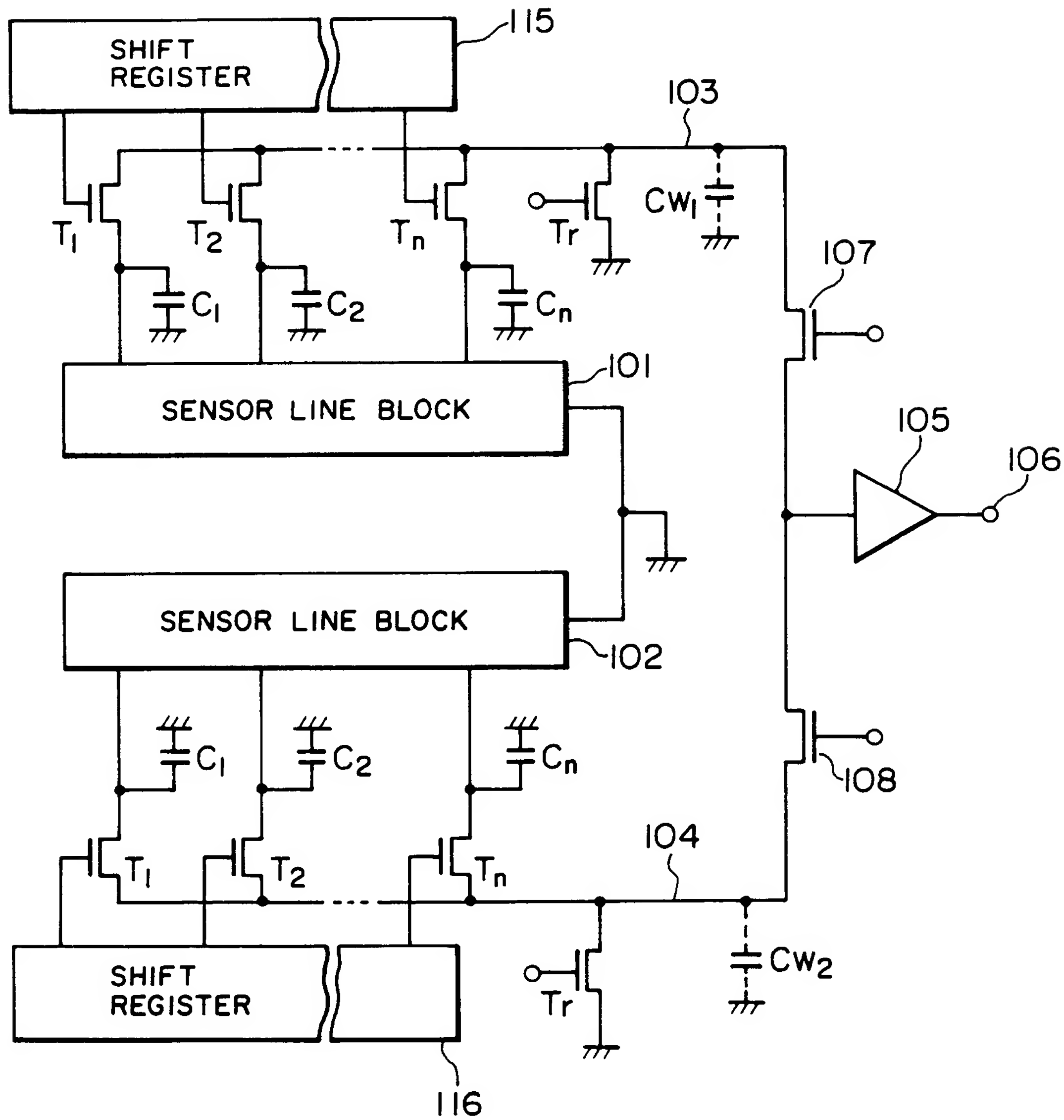

SHIFT REGISTER
115
103
T1
T2
Tn
Tr
CW1
107
C1
C2
Cn
SENSOR LINE BLOCK
101
105
106
SENSOR LINE BLOCK
102
C1
C2
Cn
108
T1
T2
Tn
104
CW2
SHIFT REGISTER
Tr
116

FIG. 2B

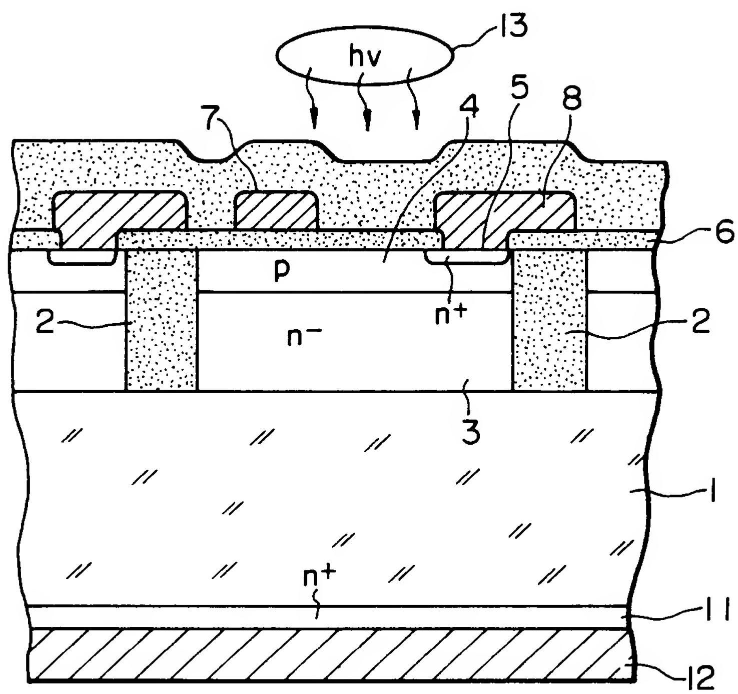


FIG. 2C

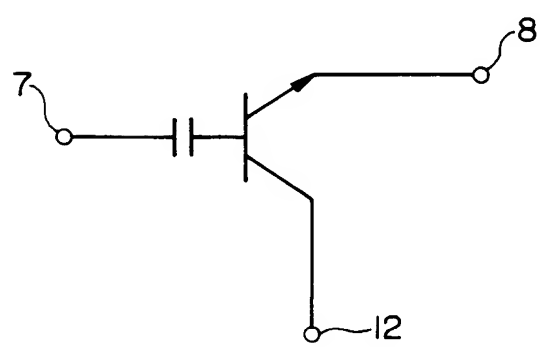


FIG. 3A

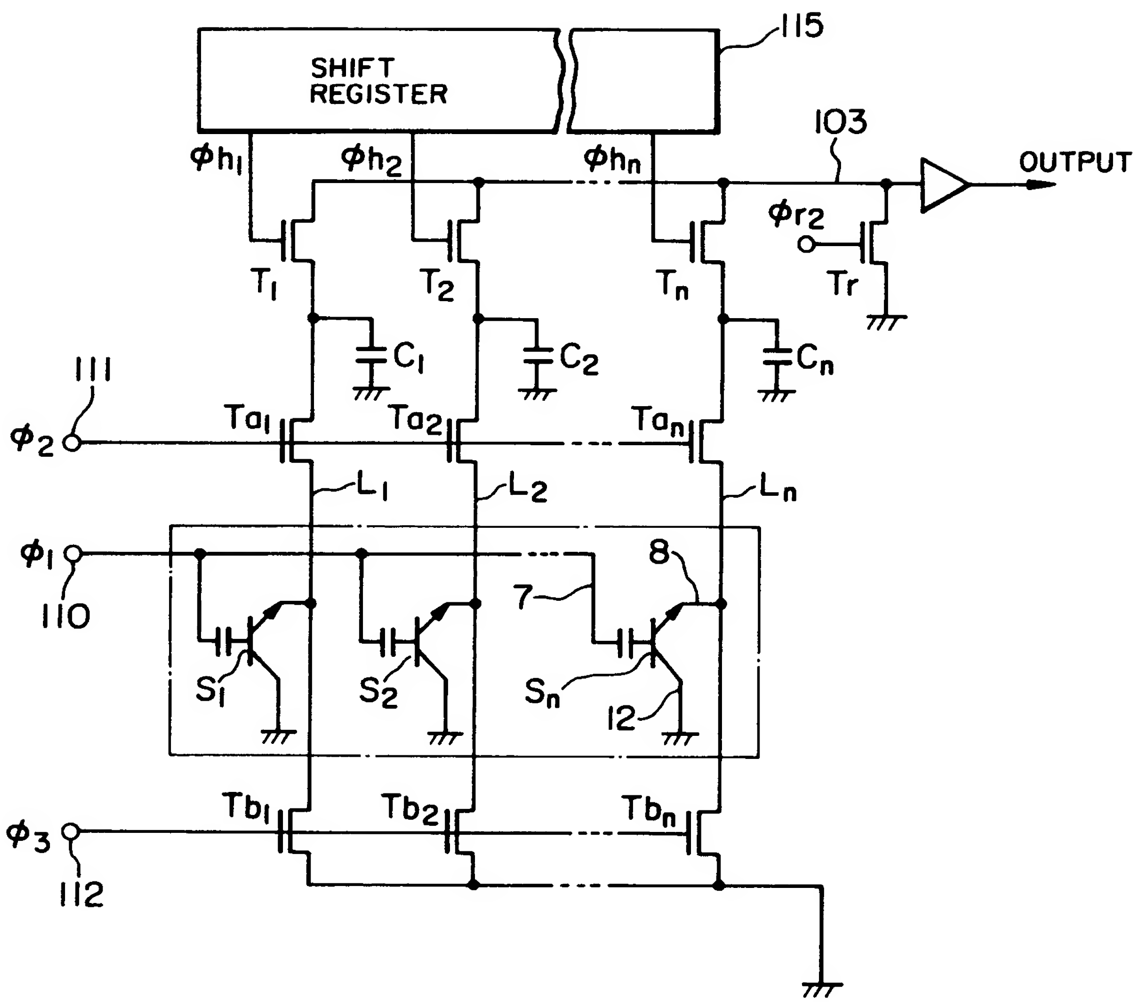

SHIFT REGISTER
115
103
OUTPUT
φh1
φh2
φhn
φr2
T1
T2
Tn
Tr
C1
C2
Cn
111
φ2
Ta1
Ta2
Tan
L1
L2
Ln
φ1
110
8
7
S1
S2
Sn
12
φ3
112
Tb1
Tb2
Tbn

FIG. 3B

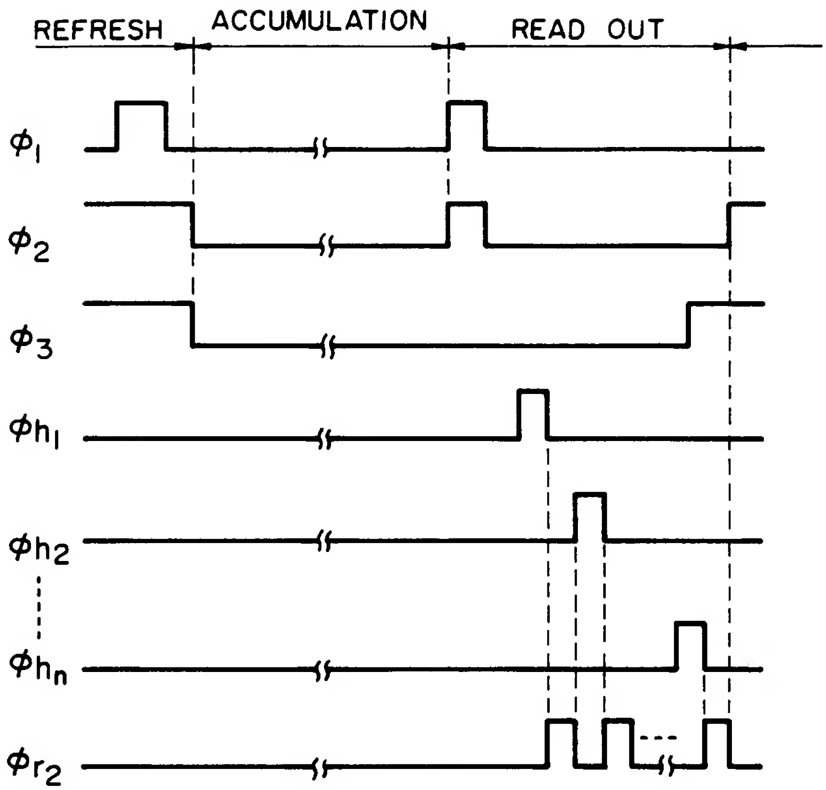

REFRESH
ACCUMULATION
READ OUT
ϕ_1
ϕ_2
ϕ_3
ϕh_1
ϕh_2
ϕh_n
ϕr_2

FIG. 4

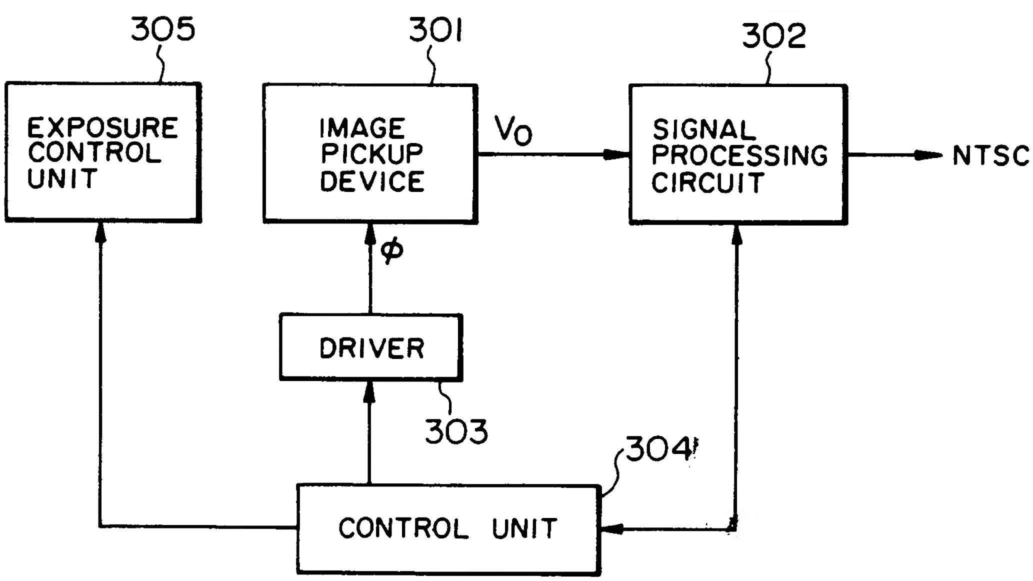

305
EXPOSURE CONTROL UNIT
301
IMAGE PICKUP DEVICE
V_O
302
SIGNAL PROCESSING CIRCUIT
NTSC
ϕ
DRIVER
303
304
CONTROL UNIT

FIG. 5

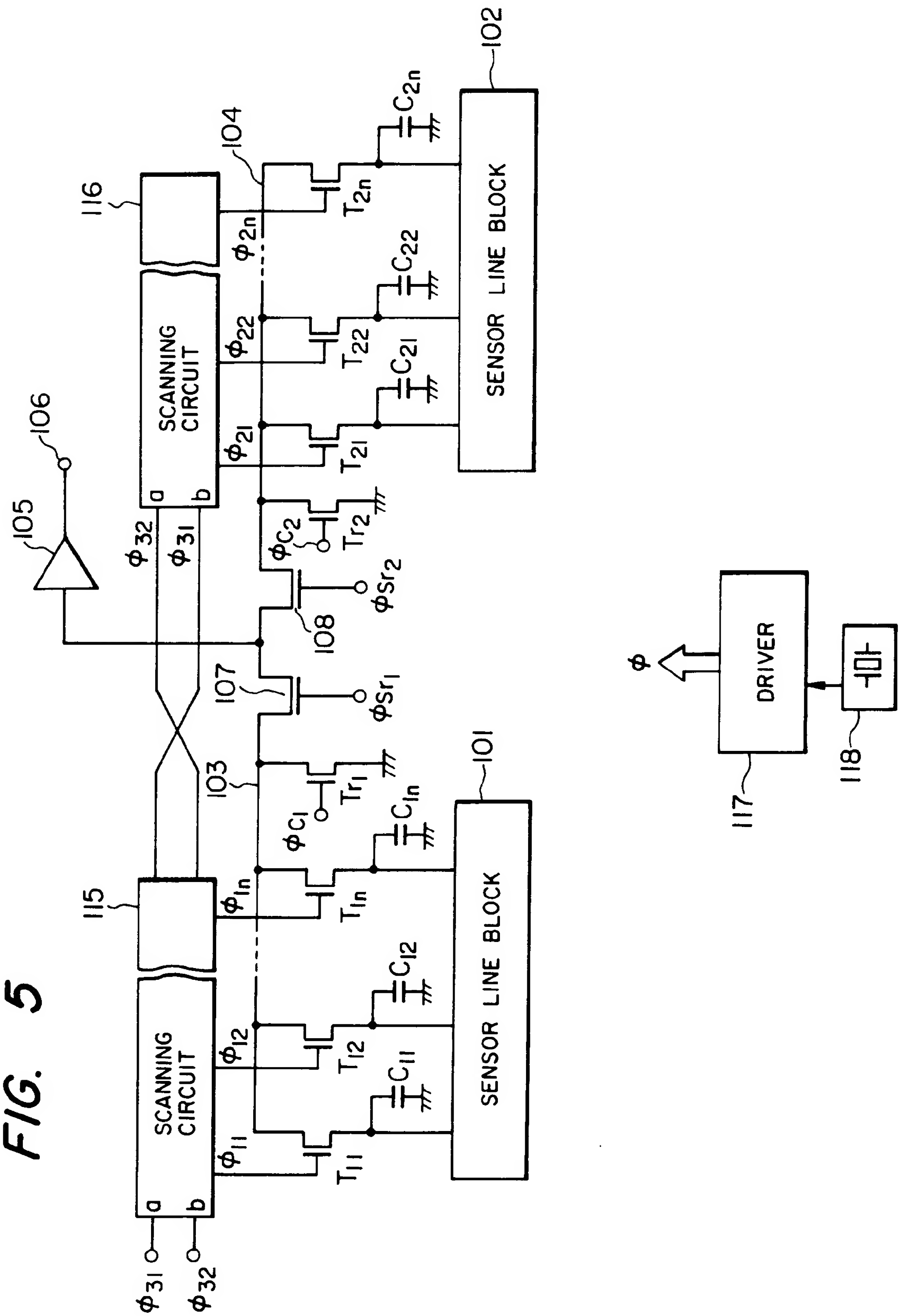

SCANNING CIRCUIT
SCANNING CIRCUIT
SENSOR LINE BLOCK
SENSOR LINE BLOCK
DRIVER
101
102
103
104
105
106
107
108
115
116
117
118
φ31
φ32
φ11
φ12
φ1n
φ21
φ22
φ2n
T11
T12
T1n
T21
T22
T2n
C11
C12
C1n
C21
C22
C2n
Tr1
Tr2
φC1
φC2
φSr1
φSr2
φ
a
b

FIG. 6

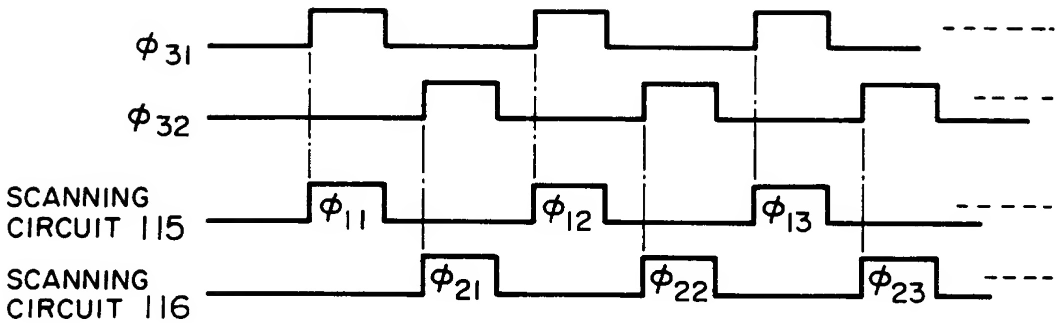
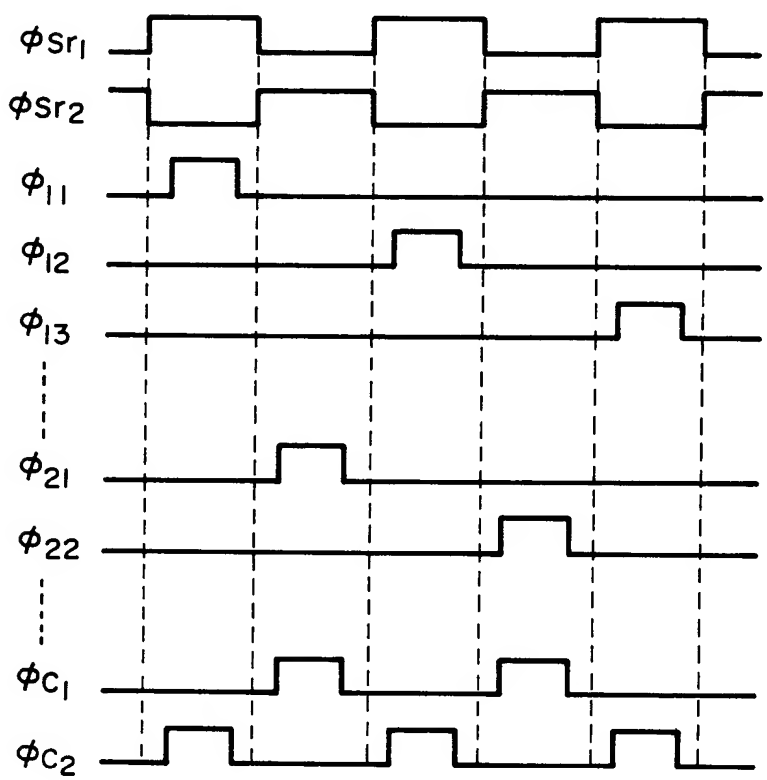

ϕ_{31}
ϕ_{32}
SCANNING CIRCUIT 115
ϕ_{11}
ϕ_{12}
ϕ_{13}
SCANNING CIRCUIT 116
ϕ_{21}
ϕ_{22}
ϕ_{23}

FIG. 7


ϕSr_1
ϕSr_2
ϕ_{11}
ϕ_{12}
ϕ_{13}
ϕ_{21}
ϕ_{22}
ϕC_1
ϕC_2